AMENDMENTS TO THE CLAIMS

1. (Previously Presented) A processor, comprising:

a selection unit, having a first input to receive a thread conditions signal indicative of one or more execution stalls, the selection unit selecting a thread from a plurality of threads based on the thread conditions signal, further comprising:

a high priority unit, having a first input coupled to the first input of the selection unit, the high priority unit selecting a thread associated with a high priority instruction from the plurality of threads,

a low priority unit, having a first input coupled to the first input of the selection unit, the low priority unit selecting a thread with a low priority instruction from the plurality of threads, and

a control mux, having a first input coupled to an output of the high priority unit and having a second input coupled to an output of the low priority unit, the control mux selecting between the high priority selection and the low priority selection; and

a selection mux, having a first input coupled to an output of the selection unit to receive the thread selection signal and a second input to receive a plurality of decoded instructions, the selection mux outputting a decoded instruction from the plurality of instructions in response to the thread selection signal.

2. (Original) The processor of claim 1, wherein the selection unit selects a thread each clock cycle.

3. (Canceled)

4. (Previously Presented) The processor of claim 1, wherein a second input to the high priority unit and a second input to the low priority unit are coupled to receive a previous thread selection, and the high priority unit and the low priority unit use round robin arbitration to select a next thread

5. (Previously Presented) The processor of claim 1, wherein the high priority unit has a third input and the low priority unit has a third input, the third high priority unit input and the third low priority unit input receiving the instruction conditions signal indicative of availability, the high priority unit selecting between threads with an available high priority instruction and the low priority unit selecting between threads with an available low priority instruction.

6. (Previously Presented) The processor of claim 1, wherein the control mux defaults to select the high priority selection.

7. (Previously Presented) The processor of claim 1, wherein the control mux selects the low priority selection after a predetermined number of successive high priority selections.

8. (Previously Presented) The processor of claim 1, wherein the thread conditions signal comprises a global stall indicator, wherein the control mux holds a selected thread responsive to an active global stall indicator.

9. (Previously Presented) The processor of claim 1, wherein the control mux selects the low priority selection if there is no high priority selection.

10. (Previously Presented) The processor of claim 1, wherein the control mux repeats a previous selection.

11. (Original) The processor of claim 1, wherein the thread conditions signal is indicative of thread eligibility, and wherein the selection unit selects between eligible threads.

12. (Original) The processor of claim 1, wherein the execution stall comprises a data cache miss.

13. (Original) The processor of claim 1, wherein the execution stall comprises an external resource stall.

14. (Original) The processor of claim 1, wherein the execution stall comprises an interlock.

15. (Original) The processor of claim 1, wherein the execution stall comprises a memory operation ordering.

16. (Original) The processor of claim 1, wherein the selection unit has a second input to receive an instruction conditions signal, the selection unit selecting a thread based on the instruction conditions signal.

17. (Original) The processor of claim 16, wherein the instruction conditions signal is indicative of one or more thread ages.

18. (Original) The processor of claim 16, wherein the instruction conditions signal is indicative of whether an instruction is available for each of the plurality of threads, and wherein the selection unit selects between available threads.

19. (Original) The processor of claim 16, wherein the instruction conditions signal comprises a priority indicator generated external to the selection unit to indicate a priority level of one or more threads.

20-68. (Canceled)